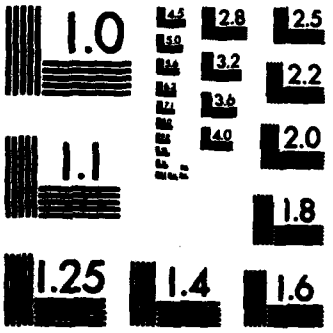
AD-A143 005 CONTINUATION OF RESEARCH IN COMPUTER SIMULATION OF INTEGRATED CIRCUITS(U) CALIFORNIA UNIV BERKELEY C O PEDERSON JUN 84 ARO-17660.4-EL DAAG29-81-K-0021 1/1

UNCLASSIFIED F/G 9/2 NL



UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

(2)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: ARO 17660.4-EL	2. GOVT ACCESSION NO.: N/A	3. RECIPIENT'S CATALOG NUMBER: N/A
TITLE (and Subtitle): Continuation of Research in Computer Simulation of Integrated Circuits		5. TYPE OF REPORT & PERIOD COVERED: 1 Nov 1980 - 30 Apr 1984 Final Report
		6. PERFORMING ORG. REPORT NUMBER
AUTHOR(s): C. O. Pederson		8. CONTRACT OR GRANT NUMBER(s): DAAG29-81-K-0021
PERFORMING ORGANIZATION NAME AND ADDRESS: Calif, Univ-Berkeley		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
CONTROLLING OFFICE NAME AND ADDRESS: U. S. Army Research Office, Post Office Box 12211, Research Triangle Park NC 27709		12. REPORT DATE: Jun 84
		13. NUMBER OF PAGES: 6
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report): Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

NA

18. SUPPLEMENTARY NOTES

The view, opinions, and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Integrated Circuits
Computerized Simulation

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Research summarized here had as its objective the investigation of emerging problems in IC simulation, including circuit equation solution, use of circuit and device model library features for hierarchical design, introduction of models for controlled switches and transmission liner into SPICE2, and development of hardware aids for circuit simulation.

AD-A143 005

DTIC FILE COPY

DTIC ELECTE JUL 13 1984 S D E

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

84 07 12 048

ARO FINAL REPORT

Introduction

The research supported by the U.S. Army Research Office under Grant DAAG29-81-K-0021 has been concerned with investigations and development activities in the simulation of integrated circuits. The research activities under this research grant commenced on November 1, 1980 and were concluded on April 30, 1984. As brought out in the following sections the results of the research have been reported in nine papers and four technical reports, in the support of six research students and in the development of several computer programs for integrated circuit simulation.

SPICE2 Program

The SPICE2 program was originally released in an engineering-use version in July 1975; the original SPICE1 program was released in May 1972. Thousands of copies of this CAD tool are now being used world wide. It is probably the most used CAD tool that presently exists. At the end of 1980, i.e., at the beginning of this ARO research grant, a new version of SPICE2 was prepared the 2G.0 version. Seven issues in this version of SPICE2 have been made during the grant period. Issue 2G.6 was released in February 1983. A number of changes and corrections have been accumulated and at the end of the grant period we are prepared to release issue 2G.7.

A charge-controlled capacitance model for MOS devices was introduced in the earlier 2F version. During an iterative solution, charge was conserved with this model. However, we found that the model employed was not easily applicable to analog circuits, particularly those operating at the middle and high frequencies. Consequently, a return to the Meyer model was made for the default case for models MOS1, 2 and 3. However, a parameter can be introduced to obtain the charge conserving capacitance, if desired.

In the latest SPICE2.G series, numerical pivoting has been introduced to reduce matrix analysis problems arising from diagonal zeros introduced during the LU decomposition due to numerical cancellation, "floating nodes" and/or from accuracy problems when large off-diagonal terms occur. It was found that full-pivoting introduced a 5 - 10% runtime increase. Consequently, an alternative pivoting scheme has been introduced to avoid the increase in CPU time while still not introducing convergent problems.

Attention is always given to transistor model improvements and aids to convergence. In addition, recent efforts have been given to investigating user-oriented I/O features. In the soon-to-be-released version, an ALTER feature will be introduced. A .ALTER statement can now be included before the parameter statements to change the values of these elements. SPICE2 automatically reruns the statement with the new values. Similarly, a .DC statement has been added. With this modification, one is able to obtain the values of a node voltage or a source current as temperature or a resistance value is swept. Other new features include RAWFILE. This enables SPICE to produce a raw data file from the results of the simulation. This raw data file can later be used by Program SPOP to display the curves of analysis interactively on a graphics terminal.

SPOP, a graphics processor for SPICE, can run on the VAX computer under the UNIX operating system using a variety of terminals. This is achieved by

including a graphics post-processor using the MFB (Model Frame Buffer) which has been implemented on the UNIX operating system. This post-processor under user control gives graphic plotting of the curves from circuit simulation. Based on MFB, SPOP is essentially graphics terminal independent. In addition, hard copies of the plotting on a Versatec or other plotter is possible once the MFB package has been extended to these machines.

Over the years, machine-code generation of several subroutines of SPICE have been used in order to obtain increased simulation speed. Within the grant period, this technique has been extended to SPICE versions for the IBM computer and for the VAX computer operating under both the VMS and the UNIX operating systems. Improvements in computer runtime of up to 30% have been obtained.

A process-oriented short-channel model (CSIM) has been implemented in SPICE2. A single process file which characterizes the fabrication process of an intergrated circuit and the layout defined by masks provide all circuit information needed by the simulation program. Several levels of the CSIM model have been installed to provide automatically increasing accuracy of the analysis as more parameters are added. A special version of SPICE is being used both locally and at a few industrial locations in order to establish any problems with the new model.

SPICE3

SPICE3 is a new circuit simulation program with all of the features of the existing SPICE2 program. However, SPICE3 is written in a format which allows it to be used more readily as a component in a larger, more comprehensive circuit-design package. In addition, it has been restructured and rewritten using macro packages and the RATFOR language to simplify maintenance and to provide ease in including future enhancements. SPICE3 retains all of the principal algorithmic routines and device model equations of SPICE2. A more recent version in the C language is also under development.

The input and output routines of SPICE2 have been completely redesigned in SPICE3 to achieve effective interactive use of the program. Circuit editing is possible and interrupt/restart capability is included. Node names are permitted and full path names to nodes within subcircuits may also be used. At the output, a sharing of post-processors with other software packages can be included, as well as the capability of dealing interactively with the output file. These I/O routines have been written in C. Finally, the interface with the device models has redesigned in order to add easily to or to change model equations and parameters.

One version of SPICE3 has been developed to work with the HAWK/SQUID CAD-IC system. HAWK is a highly developed interactive graphical input system for schematic entry and capture of various forms while SQUID is the data management system evolved for the CAD system.

In another version of SPICE3, used for the checking out of the internal algorithmic aspects, an interface has been written which reads SPICE2-type input images and produces a raw SPICE output file. A complete implementation of an interface package is under development so that SPICE3 can be a completely stand-alone program which can replace SPICE2.

SPICE3 has been tested with the full set of SPICE2 benchmark circuits of the VAX 11/780 computer running under the UNIX operating system. The execution speeds of SPICE3 are better than those of SPICE2 under the same conditions for all of the benchmark circuits.

Program SPUDS

The decreasing costs of minicomputers, coupled with recent improvements in performance, may make these machines ideal to meet the circuit simulation needs of the integrated circuit (IC) designer. An investigation has been made concerning the performance limits of circuit-level IC simulation on a dedicated microprogrammable microcomputer system.

Two types of factors limit simulation performance. First, extended precision (usually 64 bits) is customarily needed and therefore used in all floating-point calculations in circuit simulators. This precision requires twice the memory and twice the execution time of single-precision arithmetic. Second, the functional units available in the computer are not used efficiently because there is not a good match between the minicomputer instruction set and the types of operations that are needed for the simulation.

This investigation shows that circuit analysis can be performed successfully with single precision (32-bit) arithmetic through the use of a combination of numerical pivoting, sparse matrix techniques, a generalization of the indefinite admittance matrix, and voltage thresholds in the algorithms controlling convergence. The use of microcode to extend the computer instruction set greatly improves simulation speed by directly and efficiently performing several of the most time-consuming portions of the analysis. These special instructions, coupled with the smaller wordsize of the minicomputer, reduce the memory requirements of the circuit simulator by as much as two-thirds compared to the memory needs on larger computers.

One result of this investigation has been the development of a new IC simulation program, SPUDS, which has been designed to obtain the best possible performance from a specific minicomputer system. The analysis results from SPUDS using a 32-bit floating-point computations for a wide range of both analog and digital, bipolar and MOSFET circuits are almost identical with solutions based on the more common 64-bit arithmetic. Overall simulation speeds of the same order as the DEC VAX 11/780 computer are achieved using a 16-bit minicomputer. Conclusions are made concerning the suitability of several microprocessor systems for circuit-level simulation. This project has led to the development of special-purpose hardware to assist in circuit simulation, as described later.

FTL Simulator

A behavioral-level simulator has been designed and written for the simulation and investigation of IC architectures. The behavioral-level description of a processor consists of a program which is then interpreted by the simulator to predict the performance of the particular architecture under investigation. The Function-to-Logic (FTL) simulator consists of 4,000 lines of FRANZ LISP code on the VAX 11/780 computer operating under the UNIX operating system.

The FTL simulator has been used to simulate the locally developed RISC microcomputer. This microcomputer consists of over 40,000 MOS transistors in a single chip realization. The FTL input description involves approximately four page of input. FTL has been used to verify the buss timing of the processor and to produce information relating to the relative usage of the major components of the chip.

A second version of the simulator, FTL2, has been used to investigate the machine architecture of the "graph engine". The computational model used by

the "graph engine" is an extension of the data-flow model. Programs for the "graph engine" are described by directed graphs. The vertices of the graphs represent functions and variables and the edges of the graphs represent communication paths. Algorithms to solve many problems in CAD, including logic simulation, fault simulation and the compaction of symbolic layouts can be described using such graphs.

Our work builds on previous data-flow and dependency-driven approaches to multiprocessor programming. Our modeling of these computer systems employed the FTL simulation language and program. As an application program, the iterated timing analysis, (ITA), relaxation-based electrical simulation scheme was chosen. Simulation predicts that a linear speed-up with the number of processors appears possible over a wide range of circuit sizes.

Multiprocessors and Special-Purpose Hardware for CAD

Design verification of VLSI circuits requires vast amounts of computation. We have investigated the use of multiprocessors and special-purpose hardware to allow accurate circuit simulation and other CAD applications to be performed at speeds 1,000 or more time faster than is currently available or currently possible on VAX-class machines. Central to this research is a highly paralleled model of computation called augmented-data-flow.

In initial work, an implementation of the iterated timing analysis relaxation-based electrical simulation algorithm was made on multiprocessors and attention was then directed to the actual multiprocessor itself. A BBN Butterfly machine was available for this research effort. The Butterfly machine consists of ten 68000 processors working together in a data-flow architecture. With this machine, earlier simulation-based results were verified and the ITA algorithm works effectively with multiprocessor machines. Of particular importance, it has been determined that a 70% efficiency can be achieved in the use of the ten processors. This indicates that very effective runtimes for CAD programs can be achieved. In particular, logic and fault simulation as well as circuit simulation can be accomplished effectively with these types of machines, and in addition, symbolic layout checking can be investigated.

Publications under ARO Grant Sponsorship

(1) D.O. Pederson, "Computer Aids in Integrated Circuits Design" Chapter 1, *Computer Design Aids for VLSI Circuits*, Ed. P. Antognetti, D.O. Pederson, H. De Man, Sijthoff & Noordhoff, pp. 1-17.

(2) A.R. Newton, D.O. Pederson, A.L. Sangiovanni, C.H. Sequin, "Design Aids for VLSI: The Berkeley Perspective", *IEEE Trans. CAS*, Vol. CAS-28, No. 7, pp. 666-680, July 1981.

(3) A.R. Newton, "Computer-Aided Design of VLSI Circuits". *Proc. IEEEE*, Vol. 69, No. 10, pp. 1189-1199, Oct. 1981.

(4) D.O. Pederson, "IC/CAD Simulation", *Proc. Custom Integrated Circuit Conference*, May 1982.

(5) A.R. Newton, "A Survey of Computer Aids for VLSI Layout", *Digest of Technical Papers*, 1982 Symposium on VLSI Technology, IEEE CAT 82-CH1822-6, pp. 72-75.

(6) A. Vladimirescu and D.O. Pederson, "Performance Limits of the CLASSIE Circuit Simulation Program", Proc. ISCAS 1982, pp. 1229 - 1232.

(7) A. Vladimirescu and D.O. Pederson, "Circuit Simulation on Vector Processors", Proc. ICCC 1982, pp. 172 - 175.

(8) J.T. Deutsch and A.R. Newton, "Data-Flow Based Behavioral-Level Simulation and Synthesis", *Proc. ICCAD 1983*, pp. 63-64.

(9) J.T. Deutsch and A.R. Newton, "A Multiprocessor Implementation of Relaxation-Based Electrical Circuits", *Proc. DAC 1984*, to be published.

Technical Reports Issued under ARO Sponsorship

(1) A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE2", *Memorandum No. UCB/ERL M80/7*, Revised Edition, October 1980.

(2) E. Cohen, "Performance Limits of Integrated Circuit Simulation on a Dedicated Microcomputer System", *Memorandum No. UCB/ERL M81/29*, May 1981.

(3) J.T. Deutsch, "Behavioral-level Simulation and Synthesis of Digital Systems," *UCB/ERL Memo M83/47*, August 1, 1983. (This is a revised version of the MS report of J. Deutsch)

(4) T. Quarles, "SPICE3", MS Report, EECS Dept., University of California, Berkeley, December 1983.

Programs Developed and Issued under ARO Grant Sponsorship

- SPICE2
- SPICE3
- SPUDS
- FTL

Research Students Supported by the ARO Grant

Degrees Obtained

E. Cohen, Ph.D., May 1981

J. Deutsch, M.S., November 1982

T. Quarles, M.S., December 1983

R. Liu, M.S., December 1983

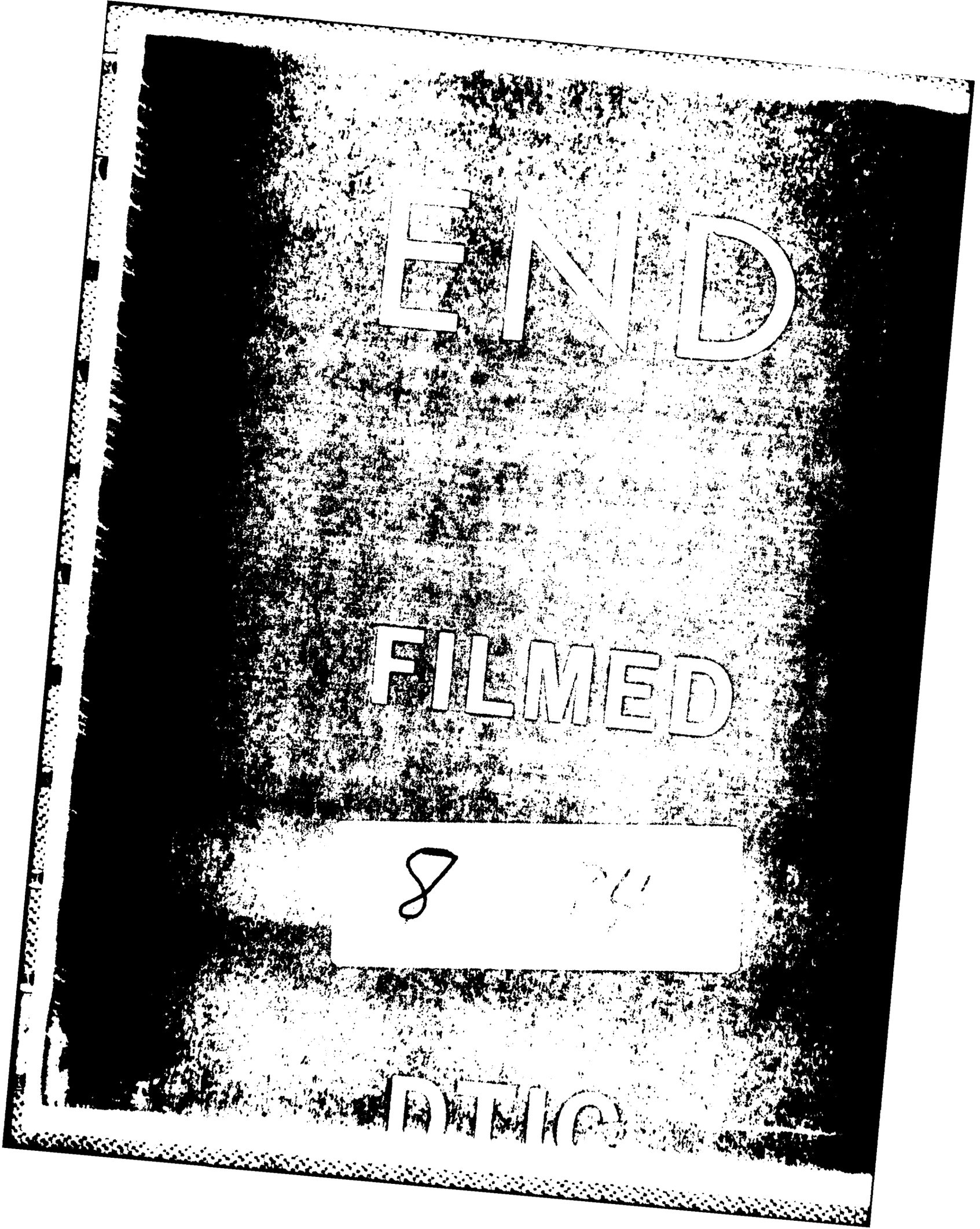
Continuing Students

D. Cheng, M.S.

W-J. Cheng, M.S.

J. Deutsch, Ph.D.

T. Quarles, Ph.D.


END
FILMED
8
DTIC